**What Is Claimed Is:**

1. A method of measuring capacitor mismatch in an analog to digital converter (ADC), said ADC converting an analog signal to a plurality of digital codes, said ADC containing a plurality of stages and a code generator, said plurality of stages being connected in sequence, a first stage contained in said plurality of stages comprising a sub-ADC, a plurality of input capacitors, an amplifier and a feedback amplifier, said sub-ADC generating a sub-code from which said code generator generates each of said plurality of digital codes, said method comprising:

sampling a first voltage on each of said plurality of input capacitors in a first phase, wherein said first voltage is designed to cause at least some of said plurality of stages to generate a sub-code equaling zero;

charging said feedback amplifier to a second voltage, wherein said second voltage is not equal to said first voltage;

connecting one of said plurality of input capacitors to said second voltage in a second phase;

connecting said feedback amplifier across said feedback amplifier in said second phase; and

determining a capacitor mismatch of said one of said plurality of input capacitors by examining a first signal generated by said second phase.

2. The method of claim 1, wherein said first voltage comprises a constant bias voltage and said second voltage comprising a reference voltage (Vref).

3. The method of claim 2, wherein said first signal comprises a digital code generated by said code generator.

4. The method of claim 3, wherein said digital code is divided by a result of multiplication of the gain of said plurality of stages except a first stage to generate a mismatch code representing said capacitor mismatch.

5. The method of claim 2, wherein the elements of claim 1 are performed in one clock cycle, said method further comprising performing the following in an earlier clock cycle, wherein said earlier clock cycle precedes said one clock cycle:

connecting all of said plurality of input capacitors and said feedback capacitor to a constant bias voltage in a first phase of said earlier clock cycle;

connecting all of said plurality of input capacitors to a constant bias voltage in a second phase of said earlier clock cycle;

connecting said feedback capacitor across said amplifier in said second phase of said earlier clock cycle; and

examining a second signal to determine an input offset presented by said plurality of stages,

wherein said capacitor mismatch is determined based on said second signal and said first signal.

6. The method of claim 5, receiving a sub-code from an intermediate stage contained in said plurality of stages, said method further comprising:

in said second phase of said one clock cycle, connecting each of a plurality of capacitors in said intermediate stage to either Vref or said constant bias voltage according to said sub-code.

7. The method of claim 6, wherein said second signal comprises a second digital code generated by said code generator, wherein said first signal comprises a first digital code generated by said code generator, wherein said capacitor mismatch is computed by subtracting said first digital code from said second digital code.

8. The method of claim 6, wherein each of said first signal and said second signal comprises an input signal provided to a last stage contained in said plurality of stages in a respective one of said early clock cycle and said one clock cycle, wherein said capacitor mismatch is computed based on a difference of voltage levels of said second signal and said first signal.

9. The method of claim 1, wherein said sampling comprises providing an INP voltage equaling an INM voltage in a differential operation, wherein a difference between said INP voltage and said INM voltage represents said first voltage.

10. An electrical circuit accurately generating a plurality of corrected codes from an analog signal, wherein said plurality of corrected codes accurately represent respective voltage levels of said analog signal, said electrical circuit comprising:

an analog to digital converter (ADC) containing a plurality of stages including a first stage, said ADC comprising:

a first stage receiving said analog signal, said first stage comprising:

a plurality of input capacitors;

an amplifier;

a feedback capacitor;

a first plurality of input switches, each of said first plurality of input switches being operable to connect a corresponding one of said plurality of input capacitors to said input signal;

a second plurality of input switches, each of said second plurality of input switches being operable to connect a corresponding one of said plurality of input capacitors to a first voltage, wherein said first voltage is designed to cause at least some of said plurality of stages to generate a sub-code equaling zero;

a third plurality of input switches, each of said third plurality of input switches being operable to connect a corresponding one of said plurality of input capacitors to a second voltage;

a fourth switch operable to connect an output terminal of said amplifier to said feedback capacitor;

a fifth switch operable to connect said feedback amplifier to said first voltage; and

a sixth switch operable to connect said feedback amplifier to said second voltage; and

a code generator block receiving each of a plurality of sub-codes from corresponding ones of said plurality of stages, and generating a digital code output; and

a calibration block controlling the operation of said first plurality of input switches, said second plurality of input switches, said third plurality of input switches, said fourth switch, said fifth switch and said sixth switch to determine a capacitor mismatch of at least one of said plurality of input capacitors.

11. The electrical circuit of claim 10, wherein said code generator block is operable to:

close said second plurality of switches to sample said first voltage on each of said input capacitors in a first phase;

close said sixth switch to charge said feedback amplifier to said second voltage;

close one of said third plurality of input switches to connect one of said plurality of input capacitors to said second voltage in a second phase; and

close said fourth switch to connect said feedback amplifier across said feedback amplifier in said second phase,

wherein said calibration block determines a capacitor mismatch of said one of said plurality of input capacitors by examining a first signal generated by said second phase.

12. The electrical circuit of claim 11, wherein said first voltage comprises a constant bias voltage and said second voltage comprising a reference voltage (Vref) used by said ADC.

13. The electrical circuit of claim 12, further comprising a correction block correcting said digital code output based on said capacitor mismatch to generate one of said plurality of corrected codes.

14. The electrical circuit of claim 13, wherein said first signal comprises a digital code generated by said code generator.

15. The electrical circuit of claim 14, wherein said digital code output is divided by a result of multiplication of the gain of said plurality of stages except a first stage to generate a mismatch code representing said capacitor mismatch.

16. The electrical circuit of claim 12, wherein the elements of claim 11 are operable in one clock cycle, said calibration block being further operable as follows in an earlier clock cycle, wherein said earlier clock cycle precedes said one clock cycle:

close said second plurality of switches and said fifth capacitor to connect all of said plurality of input capacitors and said feedback capacitor to said constant bias voltage in a first phase of said earlier clock cycle;

close said second plurality of switches to connect all of said plurality of input capacitors to said constant bias voltage in a second phase of said earlier clock cycle;

close said fourth switch to connect said feedback capacitor across said amplifier in said second phase of said earlier clock cycle; and

examine a second signal to determine an input offset presented by said plurality of

stages,

wherein said capacitor mismatch is determined based on said second signal and said first signal.

17. The electrical circuit of claim 16, wherein said calibration block is further operable to:

receive a sub-code from an intermediate stage contained in said plurality of stages;

in said second phase of said one clock cycle, connect each of a plurality of capacitors in said intermediate stage to either a reference voltage (Vref) or said constant bias voltage according to said sub-code.

18. The electrical circuit of claim 17, wherein said second signal comprises a second digital code generated by said code generator, wherein said first signal comprises a first digital code generated by said code generator, wherein said capacitor mismatch is computed by subtracting said first digital code from said second digital code.

19. The electrical circuit of claim 17, wherein said correction block correcting said digital code output by adding (said second digital code - said first digital code) to said digital code output.

20. The electrical circuit of claim 17, wherein each of said first signal and said second signal comprises an input signal provided to a last stage contained in said plurality of stages in a respective one of said early clock cycle and said one clock cycle, wherein said capacitor

mismatch is computed based on a difference of voltage levels of said second signal and said first signal.

21. The electrical circuit of claim 10, wherein said sampling comprises providing an INP voltage equaling an INM voltage in a differential operation, wherein a difference between said INP voltage and said INM voltage represents said first voltage.

22. An apparatus generating a plurality of corrected codes accurately representing the voltage levels on an analog signal, said apparatus comprising:

an analog to digital converter (ADC) converting said analog signal to a plurality of digital codes, said ADC containing a plurality of stages and a code generator, said plurality of stages being connected in sequence, a first stage contained in said plurality of stages containing a sub-ADC, a plurality of input capacitors, an amplifier and a feedback amplifier, said sub-ADC generating a sub-code from which said code generator generates each of said plurality of digital codes;

means for sampling a first voltage on each of said plurality of input capacitors in a first phase, wherein said first voltage is designed to cause at least some of said plurality of stages to generate a sub-code equaling zero;

means for charging said feedback amplifier to a second voltage, wherein said second voltage is not equal to said first voltage;

means for connecting one of said plurality of input capacitors to said second voltage in a second phase;

means for connecting said feedback amplifier across said feedback amplifier in said

second phase; and

means for determining a capacitor mismatch of said one of said plurality of input capacitors by examining a first signal generated by said second phase.

23. The apparatus of claim 22, wherein said first voltage comprises a constant bias voltage and said second voltage comprising a reference voltage (Vref).

24. The apparatus of claim 23, wherein said first signal comprises a digital code generated by said code generator.

25. The apparatus of claim 24, wherein said digital code is divided by a result of multiplication of the gain of said plurality of stages except a first stage to generate a mismatch code representing said capacitor mismatch.

26. The apparatus of claim 23, wherein the elements of claim 1 are operated in one clock cycle, said apparatus further comprising the following to operate in an earlier clock cycle, wherein said earlier clock cycle precedes said one clock cycle:

means for connecting all of said plurality of input capacitors and said feedback capacitor to a constant bias voltage in a first phase of said earlier clock cycle;

means for connecting all of said plurality of input capacitors to a constant bias voltage in a second phase of said earlier clock cycle;

means for connecting said feedback capacitor across said amplifier in said second phase of said earlier clock cycle; and

means for examining a second signal to determine an input offset presented by said plurality of stages,

wherein said capacitor mismatch is determined based on said second signal and said first signal.

27. The apparatus of claim 26, further comprising:

means for receiving a sub-code from an intermediate stage contained in said plurality of stages

in said second phase of said one clock cycle, connecting each of a plurality of capacitors in said intermediate stage to either said Vref or said constant bias voltage according to said sub-code.

28. The apparatus of claim 27, wherein said second signal comprises a second digital code generated by said code generator, wherein said first signal comprises a first digital code generated by said code generator, wherein said capacitor mismatch is computed by subtracting said first digital code from said second digital code.

29. The apparatus of claim 27, further comprises means for correcting to add (said second digital code - said first digital code) to each of said plurality of digital codes generated by said ADC.

30. The apparatus of claim 27, wherein each of said first signal and said second signal comprises an input signal provided to a last stage contained in said plurality of stages in a

respective one of said early clock cycle and said one clock cycle, wherein said capacitor mismatch is computed based on a difference of voltage levels of said second signal and said first signal.

31. The apparatus of claim 23, wherein said sampling comprises providing an INP voltage equaling an INM voltage in a differential operation, wherein a difference between said INP voltage and said INM voltage represents said first voltage.

32. A device processing an analog signal, said device comprising:

an analog to digital converter (ADC) containing a plurality of stages including a first stage, said ADC comprising:

a first stage receiving said analog signal, said first stage comprising:

a plurality of input capacitors;

an amplifier;

a feedback capacitor;

a first plurality of input switches, each of said first plurality of input switches being operable to connect a corresponding one of said plurality of input capacitors to said input signal;

a second plurality of input switches, each of said second plurality of input switches being operable to connect a corresponding one of said plurality of input capacitors to a first voltage, wherein said first voltage is designed to cause at least some of said plurality of stages to generate a sub-code equaling zero;

a third plurality of input switches, each of said third plurality of input switches being operable to connect a corresponding one of said plurality of input capacitors to a second voltage;

a fourth switch operable to connect an output terminal of said amplifier to said feedback capacitor;

a fifth switch operable to connect said feedback amplifier to said first voltage; and

a sixth switch operable to connect said feedback amplifier to said second voltage; and

a code generator block receiving each of a plurality of sub-codes from corresponding ones of said plurality of stages, and generating an uncorrected code; and

a calibration block controlling the operation of said first plurality of input switches, said second plurality of input switches, said third plurality of input switches, said fourth switch, said fifth switch and said sixth switch to determine a capacitor mismatch of at least one of said plurality of input capacitors.

33. The device of claim 32, wherein said code generator block is operable to:

close said second plurality of switches to sample said first voltage on each of said input capacitors in a first phase;

close said sixth switch to charge said feedback amplifier to said second voltage in said first phase;

close one of said third plurality of input switches to connect one of said plurality of

input capacitors to said second voltage in a second phase; and

close said fourth switch to connect said feedback amplifier across said feedback amplifier in said second phase,

wherein said calibration block determines a capacitor mismatch of said one of said plurality of input capacitors by examining a first signal generated by said second phase.

34. The device of claim 33, wherein said first voltage comprises a constant bias voltage and said second voltage comprising a reference voltage (Vref) used by said ADC.

35. The device of claim 34, further comprising a correction block correcting said uncorrected code based on said capacitor mismatch to generate one of said plurality of digital codes.

36. The device of claim 35, wherein said first signal comprises a digital code generated by said code generator.

37. The device of claim 36, wherein said digital code is divided by a result of multiplication of the gain of said plurality of stages except a first stage to generate a mismatch code representing said capacitor mismatch.

38. The device of claim 34, wherein the elements of claim 11 are operable in one clock cycle, said calibration block being further operable as follows in an earlier clock cycle, wherein said earlier clock cycle precedes said one clock cycle:

close said second plurality of switches and said fifth capacitor to connect all of said plurality of input capacitors and said feedback capacitor to said constant bias voltage in a first phase of said earlier clock cycle;

close said second plurality of switches to connect all of said plurality of input capacitors to said constant bias voltage in a second phase of said earlier clock cycle;

close said fourth switch to connect said feedback capacitor across said amplifier in said second phase of said earlier clock cycle; and

examine a second signal to determine an input offset presented by said plurality of stages,

wherein said capacitor mismatch is determined based on said second signal and said first signal.

39. The device of claim 38, wherein said calibration block is further operable to:

receive a sub-code from an intermediate stage contained in said plurality of stages;

in said second phase of said one clock cycle, connect each of a plurality of capacitors in said intermediate stage to either a reference voltage (Vref) or said constant bias voltage according to said sub-code.

40. The device of claim 39, wherein said second signal comprises a second digital code generated by said code generator, wherein said first signal comprises a first digital code generated by said code generator, wherein said capacitor mismatch is computed by subtracting said first digital code from said second digital code.

41. The device of claim 39, wherein each of said first signal and said second signal comprises an input signal provided to a last stage contained in said plurality of stages in a respective one of said early clock cycle and said one clock cycle, wherein said capacitor mismatch is computed based on a difference of voltage levels of said second signal and said first signal.

42. The device of claim 32, wherein an INP voltage equaling an INM voltage is provided in a differential operation, wherein a difference between said INP voltage and said INM voltage represents said first voltage.

43. The device of claim 32, wherein said device comprises a wireless base station.